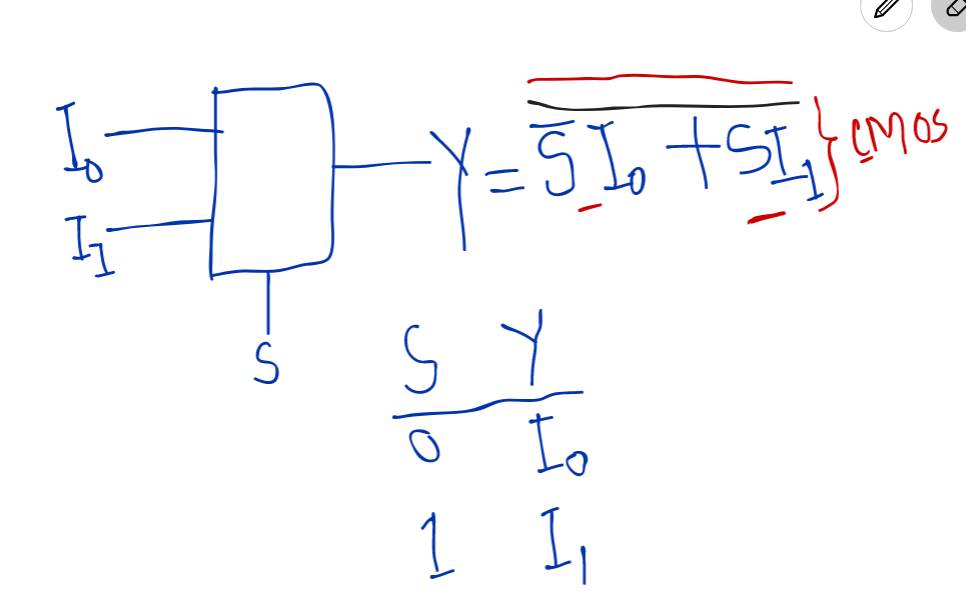
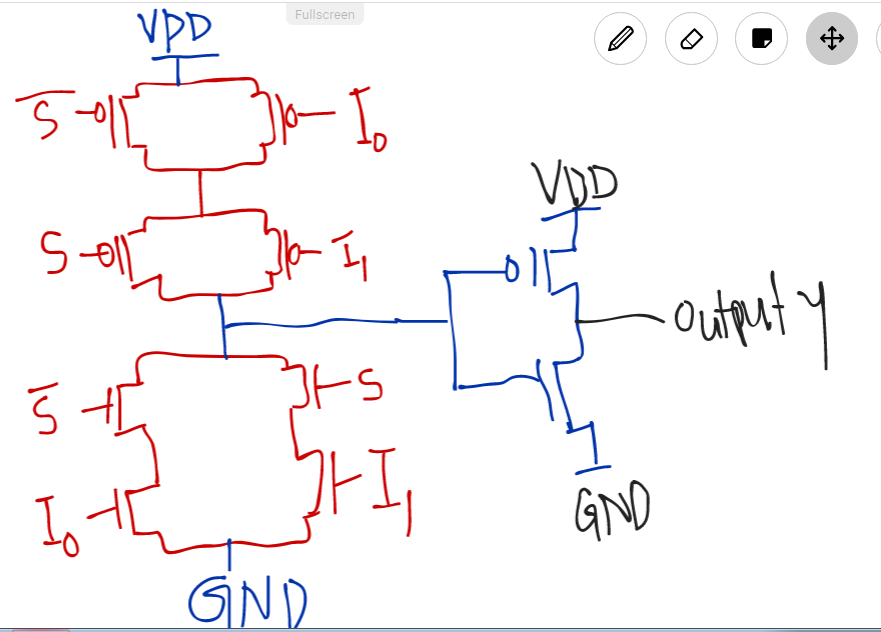
1. Design CMOS Equivalent circuit of a 2:1 MUX/Multiplexer.





Input n….select switch s….

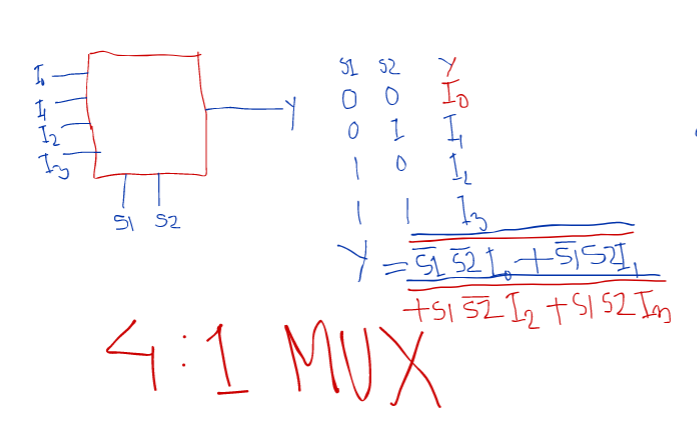
S = log2n

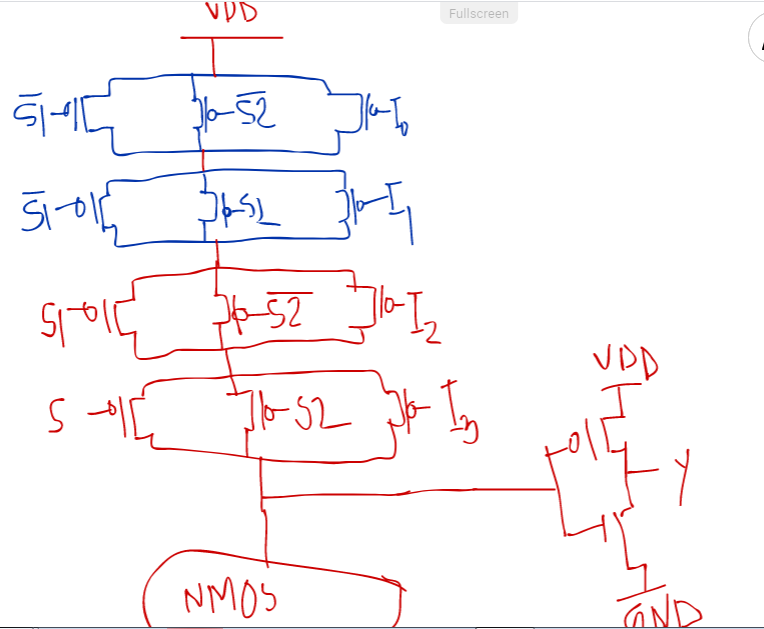
N = 2….s = log22 = 1

N = 4….s = log24 = log222 = 2 log22 = 2

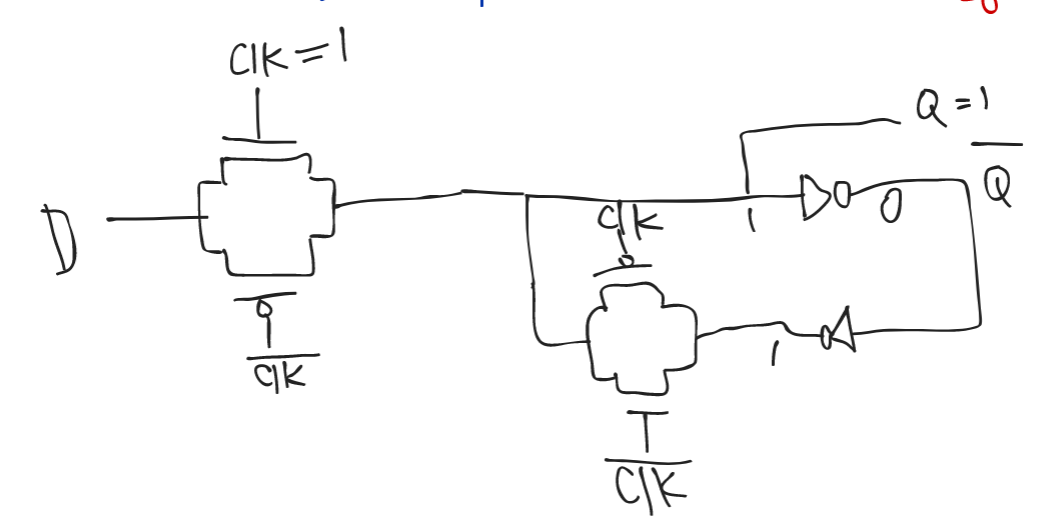
N = 16….s = log216 = log224 = 4

1. Design CMOS Equivalent circuit of a 4:1 MUX/Multiplexer.





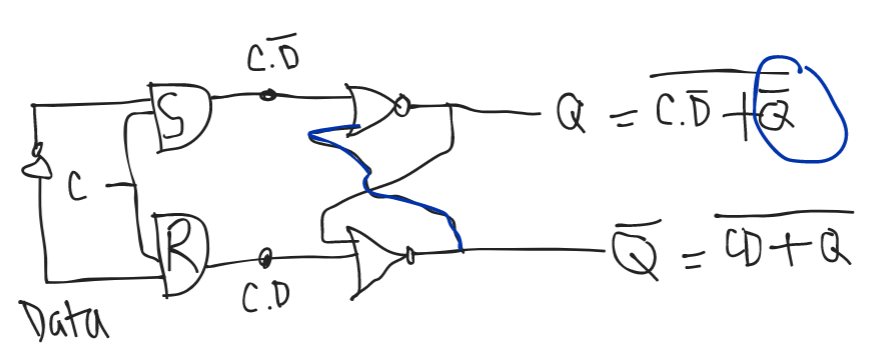
1. Design D latch using MUX.



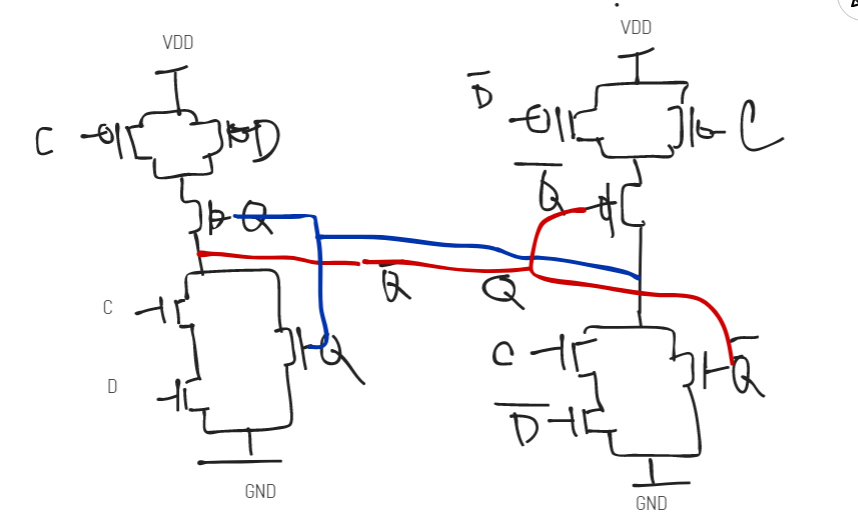
1. Relationship among D, Q and clock in a D latch.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Clock | 0 | 0 | 1 | 1 | 0 | 0 |
| D | 0 | 1 | 1 | 0 | 1 | 0 |
| Q | 0 | 0 | 1 | 0 | 0 | 0 |

1. Design D latch using logic gate.



1. Show the CMOS Implementation of D latch.



1. Table of input for D flip flop…D,Q and clock relationship show.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Clk | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| D | 1 | 1 | 0/1 - X | 0/1 - X | 0/1 – X | 0 | 0 |
| Q | 0 | 0 | 1 | 1 | 1 | 1 | 0 |